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Single-phase multilevel inverter topologies with self-voltage balancing capabilities

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Abstract: In this study, two new structures of single-phase hybrid multilevel inverter are proposed for both symmetrical and asymmetrical configurations that can be employed in drives and control of electrical machines and connection of renewable energy sources. The proposed configuration uses a less number of semiconductor devices and DC sources as compared with conventional and newly developed topologies which lead to a reduction in cost and installation area. The proposed topology poses a vital advantage of self-voltage balancing of its capacitor voltage regardless of load type, load dynamics and modulation index. Also, the proposed topology is expanded in a cascaded fashion which reduces the complexity and improves the performance significantly. A wide range of comparison is done with conventional and newly developed topologies to show the superior performance of proposed topologies regarding a total number of switches and DC sources. The multi-carrier pulse-width modulation strategy is adopted for generating switching pulses for respective switches. A laboratory prototype is developed for testing the performance of the proposed topology for 9-level and 17-level inverters.

1 Introduction

Multilevel inverter (MLI) provides the solution to overcome the voltage restriction of the classical 2-level inverter and to reach the higher power level by using a series connection of various semiconductor devices with suitable control technique. The first MLI topology was introduced about four decades ago, and since then huge thrust is seen in the field of power converters and their applications [1–3]. MLI is employed in high power applications such as AC motor drive [4, 5], active power filters [6, 7] and integration of renewable energy into the grid [8, 9]. Apart from high-voltage compatibility, MLI also poses supplementary benefits such as improved power quality, reduced total harmonic distortion, less voltage stress across the switches, good electromagnetic compatibility, reduced switching losses and dv/dt stress.

Traditionally, MLIs are classified into three categories, and they are: cascaded H-bridge (CHB), flying capacitor (FC) and neutral point clamped (NPC) and these topologies are widely referred to as 'Classical Topologies' [10, 11]. However, the classical topologies have several constraints, i.e. for a higher number of output levels (>5), the number of DC sources and switches are increased which also increase peripheral devices such as gate driver circuit, protection circuit and heat sink. This increment in the components leads to increase in cost, overall system complexity, losses and reduces the reliability and efficiency of the converter. Hence, along with the exploration of classical topologies, a substantial thrust is seen in the evolution of application-oriented newer topologies with a reduced number of devices [12–14] and their modulation/control techniques [15, 16] in the last decade.

The topology of [17] presents a configuration of cascaded MLI which utilises sub-MLI units, but it requires large amounts of bidirectional switches which increase the losses in the proposed topology as compared with conventional CHB. Moreover, the proposed topology cannot be operated in an asymmetrical mode, hence lags behind conventional asymmetrical CHB. The topology of [18] initially proposes sub-MLI, and then for achieving a maximum number of output levels in asymmetrical configuration, the cascaded structure has been proposed. It requires a different variety of switches regarding blocking voltage capabilities which increase the cost and complexity of the converter. Moreover, the power balancing among different input sources is not possible and consequently life is reduced. The topologies of [19, 20] use the series connection of DC sources. Also, a cascaded structure is proposed for obtaining the maximum number of levels in output. It requires a large number of bidirectional switches which increases the overall losses of the proposed inverter. The topologies of [17–20] suffer from one major drawback, i.e. the switches of its H-bridge have to bear the total input voltage which restricts the operation at higher-voltage levels. The topologies of [21–23] propose inverter which reduces switches significantly when compared with conventional CHB. However, both binary and trinary combinations of DC sources for the asymmetrical operation of the proposed topologies are not possible due to which it lags behind the conventional CHB.

In [24], a symmetrical topology of MLI is proposed which reduces the number of components and has a simple modulation scheme. Switches of its H-bridge have to bear the full rated voltage of the inverter which restricts its application at high-voltage levels which is a major disadvantage. In [18], another topology for MLI is proposed, but the main drawbacks for this topology are the use of bidirectional switches, a variety of switches and restriction on high-voltage applications. In [25], another symmetrical MLI topology has been proposed using less number of switches and reducing the switching losses up to a great extent as compared with conventional MLI. However, a major drawback is the loss of its modularity. The topologies of [26, 27] require more switches as compared with the proposed topology. In [28], topologies have been presented for both symmetrical and asymmetrical MLIs, but the main drawback is the range of available power factor being very narrow; only loads with power factor close to unity can be supplied. In [29, 30], two topologies based on developed H-bridges are introduced. The main drawback of these topologies is the requirement of a large number of independent DC sources which increases the cost of these topologies. From the above literature, it is concluded that, to achieve a higher number of output levels with a less number of devices, great compromise has been made in terms of number of bidirectional switches, unidirectional switches, DC sources, variety of switches, variety of heat sinks, variety of DC sources, reliability, modularity, simplicity, flexibility and switching losses. The concern mentioned above has been scaled down to a great extent in the proposed topologies.

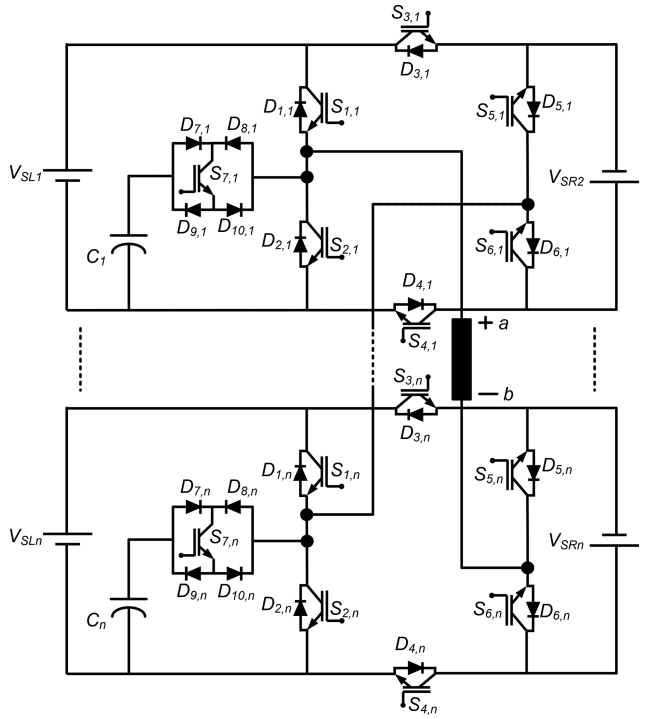

Fig. 1 *Configuration of the proposed topology-I*

Table 1 Switching table for 9-level inverter of topology-I

Output levels	'ON' state switches	Effect on capacitor voltage	
		If 'i_L>0'	If 'i_L<0'
C_V	S_4, S_6, S_7	discharging	charging
V_{SR}	S_2,S_4, S_5	no effect	no effect
$C_V + V_{SR}$	S_4, S_5, S_7	discharging	charging
$V_{SL} + V_{SR}$	S_1, S_4, S_5	no effect	no effect
0 V	S_2, S_4, S_6	no effect	no effect
$-C_V$	S_3, S_5, S_7	discharging	charging
$-V_{SR}$	S_1, S_3, S_6	no effect	no effect
$-(V_{SL} + V_{SR} - C_V)$	S_3, S_6, S_7	discharging	charging
$-(V_{SL} + V_{SR})$	S_2, S_3, S_6	no effect	no effect

A symmetrical topology is presented in [31] which uses single DC source in parallel of series-connected capacitors. The main disadvantage of this topology is that only symmetrical configuration is given. Moreover, four of its switches have to bear the total voltage of the inverter restricting its application to medium voltage. The topology of [32] proposes a cascaded version of the topology of [31] that can be operated at high-voltage levels as the sub-blocks are connected in a cascaded manner. In [33], the topology of [31] has been modified to asymmetrical version to reach a maximum number of output levels. Implementation of many bidirectional switches is the main drawback of this topology. In [34], the topology of [31] has been presented for both symmetrical and asymmetrical MLIs which reach a higher number of output levels. The main drawback is the requirement of a large number of independent DC source which increases its cost tremendously.

In [35], another topology of the MLI is proposed for 5-level inverter using single DC source and two CHB configurations. In this topology, capacitor voltage of one of the CHB blocks is regulated by a phase shift modulation technique which reduces the number of isolated DC sources by half amount. The main limitation of this topology is that the switches of its main H-bridge have to block the total output voltage of the inverter which restricts its application in higher-voltage application. The topologies of [36–39] propose packed U-cell topology which reduces the number of isolated DC sources by a large margin compared with conventional CHB. The main advantage of these topologies is that they do not require any external circuitry for maintaining its capacitor voltage in a balanced state. In [40], a new switching strategy is developed by combining selective harmonic mitigation and selective harmonic elimination techniques for four leg NPC inverter which not only reduces the power losses, but also maintains the DC capacitors voltage in a balanced state with low-voltage ripples even at lower switching frequencies. The topology of [41, 42] proposes topologies of MLI that reduces the DC source requirement by using capacitors without the assistance from an external circuit, i.e. the topologies of [41, 42] have self-voltage balancing capabilities, but both topologies require a large number of switches as compared with proposed topologies.

In this paper, two new topologies are presented which can be operated in both symmetrical as well as asymmetrical configurations. The proposed topology has a modular structure as it is connected in a cascaded fashion and provides reliable operation for symmetrical and asymmetrical configurations with less voltage stress on the semiconductor switches. It does not require any external circuit for balancing its capacitor voltage due to its self-voltage balancing capability. 'Self-voltage balancing' means the ability of the capacitor to maintain its voltage in a balanced state without requiring any aid from the external circuit irrespective of load dynamics, modulation index or transients. The symmetrical and asymmetrical configurations of proposed topologies generate the maximum number of output levels with less number of switches and isolated DC sources comparatively. The number of bidirectional switches also reduces significantly in the proposed topologies. The proposed topologies also have added the advantage of equal DC source utilisation and reduced losses. A detailed comparison of proposed topologies with classical topologies and some recently newly developed topologies is done based on the number of switches and DC sources for both symmetrical and asymmetrical configurations to effectively show the benefits of the proposed topology.

2 Proposed MLI topologies

2.1 Proposed topology-I:

The generalised configuration of topology-I in a symmetrical configuration is shown in Fig. 1. Each cell in topology-I is composed of seven controlled switches, ten power diodes, two DC sources and one capacitor. The DC source on the left-hand side is numbered as V_{SL1}, V_{SL2}, …, V_{SLn} and on the right-hand side is numbered as V_{SR1}, V_{SR2}, …, V_{SRn} ('n denotes the number of series cell').

The generalised mathematical expression for topology-I in the symmetrical configuration for 'N' cells

$$\text{number of DC sources} = 2N \tag{1}$$

$$\text{number of capacitors} = N \tag{2}$$

$$\text{number of IGBT's} = 7 \times N \tag{3}$$

$$\text{number of diodes} = 10 \times N \tag{4}$$

$$\text{number of output levels} = (8 \times N + 1) \tag{5}$$

Switching scheme for 9-level of topology-I is given in Table 1 along with the capacitor charging and discharging states. It has to be noted that for pure resistive load, the capacitor discharges at voltage levels 'C_V' and '$C_V + V_{SR}$', whereas charging of capacitor takes place at voltage level '$-C_V$' and '$(V_{SL} + V_{SR} - C_V)$'. No other states can affect the capacitor voltages. Fig. 2 demonstrates the flow of current at all the respective levels.

2.2 Proposed topology-II

For asymmetrical operation, the proposed topology-I is slightly modified by adding one extra bidirectional switch and a capacitor

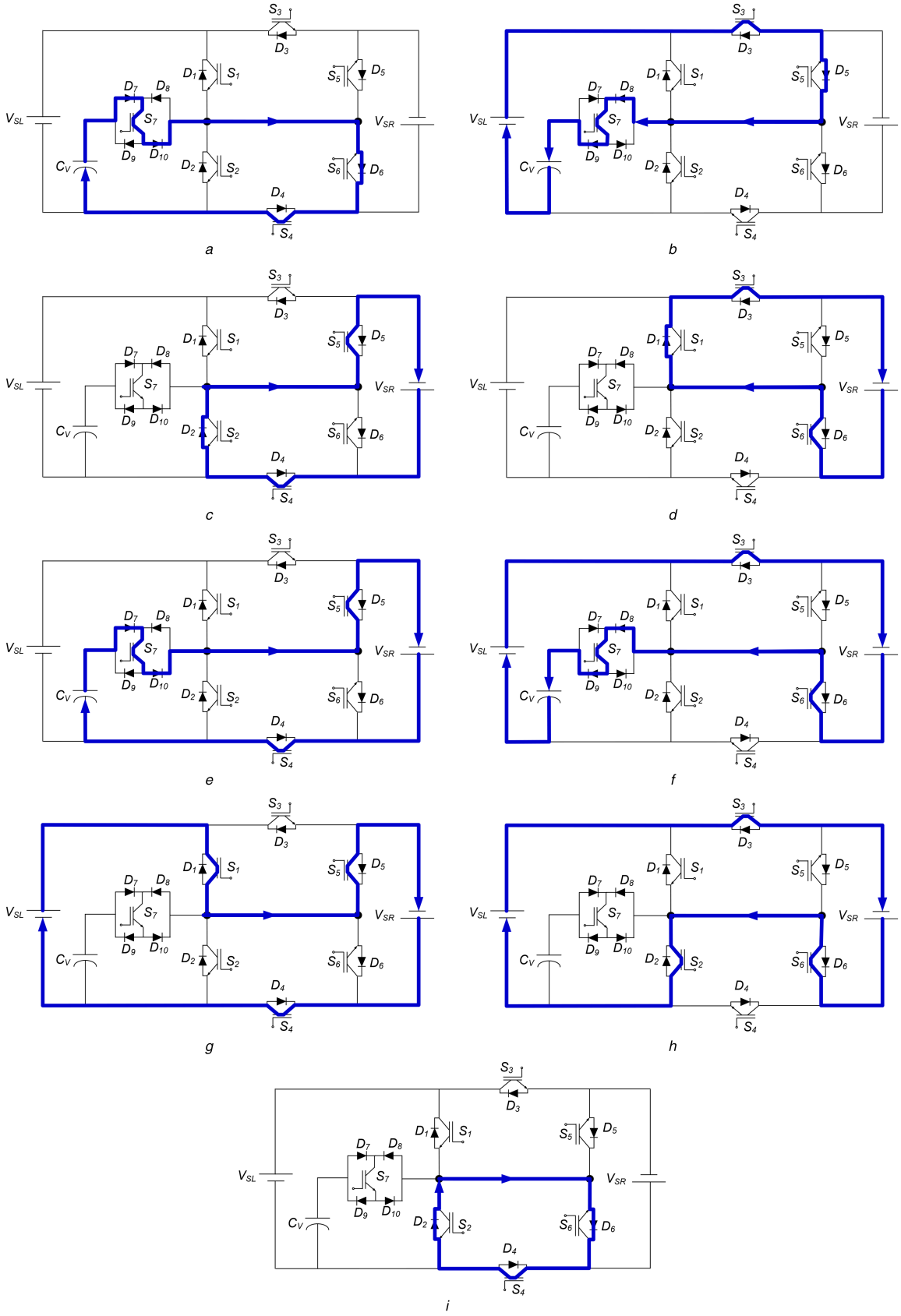

Fig. 2 *Current flow direction of topology-I for 9-level output*

(a) Output voltage = C_V, ***(b)*** Output voltage = $-(V_{SL}-C_V)$, ***(c)*** Output voltage = V_{SR}, ***(d)*** Output voltage = $-V_{SR}$, ***(e)*** Output voltage = $(V_{SR}+C_V)$, ***(f)*** Output voltage = $-(V_{SR}+V_{SL}-C_V)$, ***(g)*** Output voltage = $(V_{SR}+V_{SL})$, ***(h)*** Output voltage = $-(V_{SR}+V_{SL})$, ***(i)*** Output voltage = 0V

in each cell, and its generalised form is given in Fig. 3 and called it as proposed topology-II. Like topology-I, the topology-II is also connected in a cascaded manner to achieve modularity. The DC source on the left-hand side is numbered as V_{SL1}, V_{SL2}, …, V_{SLn} and on the right-hand side is numbered as V_{SR1}, V_{SR2}, …, V_{SRn}. It can also be operated as symmetrical configuration by using the same values of DC sources. Table 2 gives the different switching states for 9-level output for the proposed topology-II. For asymmetrical operation, the values of DC sources are assigned according to Table 3. In conventional asymmetrical CHB, the

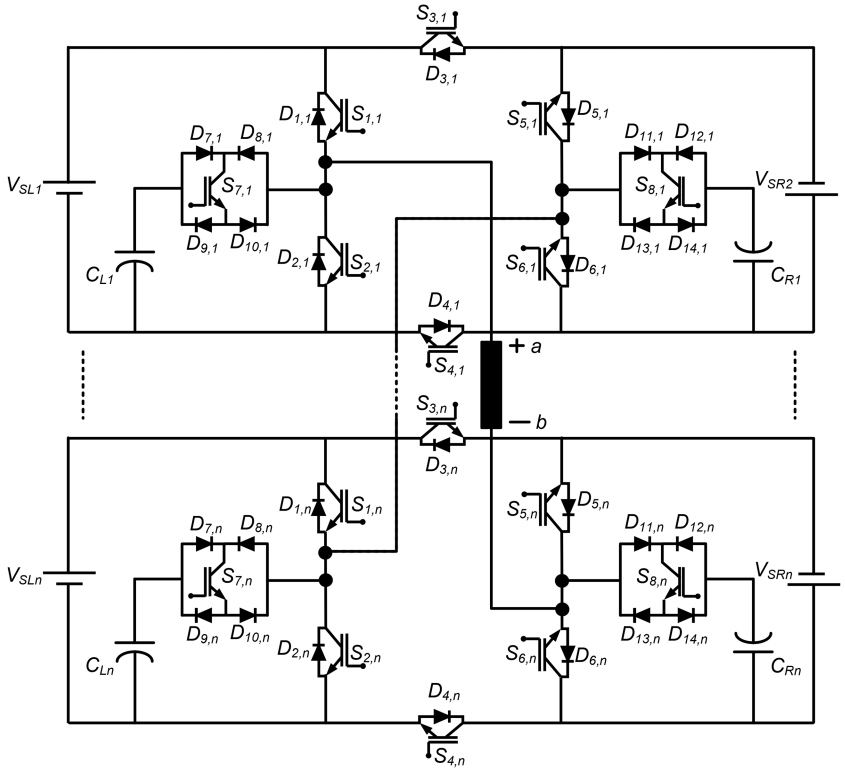

Fig. 3 *Configuration of the proposed topology-II*

Table 2 Switching table for 9-level inverter of topology-II

Output Levels	'ON' state switches	Effect on capacitor voltage			
		Capacitor C_L		Capacitor C_R	
		If '$i_L > 0$'	If '$i_L < 0$'	If '$i_L > 0$'	If '$i_L < 0$'
C_L	S_4, S_6, S_7	discharging	charging	no effect	no effect
$C_L + C_R$	S_4, S_7, S_8	discharging	charging	discharging	charging
$C_L + V_{SR}$	S_4, S_5, S_7	discharging	charging	no effect	no effect
$V_{SL} + V_{SR}$	S_1, S_4, S_5	no effect	no effect	no effect	no effect
0 V	S_2, S_4, S_6	no effect	no effect	no effect	no effect
$-(V_{SL} - C_L)$	S_3, S_5, S_7	discharging	charging	no effect	no effect
$-(V_{SL} + V_{SR} - C_L - C_R)$	S_3, S_7, S_8	discharging	charging	discharging	charging
$-(V_{SL} + V_{SR} - C_L)$	S_3, S_6, S_7	discharging	charging	no effect	no effect
$-(V_{SL} + V_{SR})$	S_2, S_3, S_6	no effect	no effect	no effect	no effect

Table 3 Realisation of different levels of proposed topology-II incorporating 'n' number of cells

Algorithm	Values of DC sources	Number of output levels	Configuration
first	$V_{SL1} = V_{SR1} = \cdots = V_{SLn} = V_{SRn}$	$8 \times n + 1$	symmetrical
second	$\frac{V_{SL1}}{2^0} = \frac{V_{SR1}}{2^1} = \frac{V_{SL2}}{2^2} = \frac{V_{SR2}}{2^3} = \cdots = \frac{V_{SLn}}{2^{2\times n-2}} = \frac{V_{SRn}}{2^{2\times n-1}}$	$4 \times \left[\sum_{m=1}^{n}(V_{SLm} + V_{SRm}) \div V_{SL1}\right] + 1$	asymmetrical
third	$\frac{V_{SL1}}{3^0} = \frac{V_{SR1}}{3^1} = \frac{V_{SL2}}{3^2} = \frac{V_{SR2}}{3^3} = \cdots = \frac{V_{SLn}}{3^{2\times n-2}} = \frac{V_{SRn}}{3^{2\times n-1}}$	$4 \times \left[\sum_{m=1}^{n}(V_{SLm} + V_{SRm}) \div V_{SL1}\right] + 1$	asymmetrical
fourth	V_{SL1} = initialise $V_{SR1} = 3 \times V_{SL1}$ $V_{SLn} = 4 \times \left[\sum_{m=1}^{n-1}(V_{SLm} + V_{SRm})\right] + V_{SL1}$ $V_{SRn} = 2 \times \left[V_{SLn} + \left(\sum_{m=1}^{n-1}(V_{SLn} + V_{SRn})\right)\right] + V_{SL1}$	$4 \times \left[\sum_{m=1}^{n}((V_{SLm} + V_{SRm}) \div V_{SL1})\right] + 1$	asymmetrical

values of DC sources are assigned in a predefined manner of either binary (2:1) or trinary (3:1) combination and accordingly the output levels increase. However, some recently published literature shows the working of asymmetrical topology by assigning values of DC sources in a predefined manner of 4:1 [33], 5:1 [33] and even 7:1 [30], due to which the number of output levels tremendously increases as compared with asymmetrical CHB. Therefore, in order to reach the highest number of output levels in the proposed topology-II, a new algorithm is adopted which is given in Table 3 (fourth algorithm).

2.3 Capacitor voltage balancing

In the proposed topology, the capacitor voltage always remains in a balanced state irrespective of the load type, modulation index or load characteristics. Also, the proposed topology does not require any complicated methods for maintaining its capacitor voltage in a balanced state.

This phenomenon can be explained mathematically by capacitor ampere-second balance equation; according to this equation, the net change in capacitor voltage over single switching cycle under steady-state condition should be zero. Current across capacitor is given by

$$i_C(t) = C\frac{dv_C(t)}{dt} \tag{6}$$

where '$i_C(t)$' is the instantaneous capacitor current and '$v_C(t)$' is the corresponding voltage across the capacitor at the same instant.

Integration of the above equation over single switching cycle yields

$$\int_0^{T_S} i_C(t)\,dt = C\int_0^{T_S}\left(\frac{dv_C(t)}{dt}\right)dt \tag{7}$$

$$\int_0^{T_S} i_C(t)\,dt = V_C(t) - V_C(0) \tag{8}$$

Now from (8), it can be said that the net change in capacitor voltage over single switching cycle is equal or proportional to integral of capacitor current over the same switching cycle. In steady state, initial and final values of capacitor voltages are the same. Therefore

$$\text{average capacitor current} = \frac{1}{T_S}\int_0^{T_S} i_C(t)\,dt = 0 \tag{9}$$

From (9), it can be concluded that the average value or DC component of the capacitor current must be zero in equilibrium. The detailed analysis of capacitor voltage balancing is presented in Fig. 4*a*.

3 Comparison studies

The proposed topology-I offers more benefits in symmetrical configuration and topology-II in an asymmetrical configuration. Therefore, in this section, a suitable comparison is drawn for topology-I in a symmetrical configuration and topology-II is compared with newly developed asymmetrical topologies.

3.1 Comparison of symmetrical MLI

Comparison of the proposed topology-I with newly developed topologies of [26, 27, 30, 32, 34] and conventional CHB operated in symmetrical configuration is given in Figs. 5*a* and *b*. It can be observed that the proposed topology-I requires the least amount of switches in a symmetrical configuration. Moreover from Fig. 5*b*, it can be seen that the DC source requirement in the proposed topology-I is less than topologies of [27, 30, 34] and equal to topologies of [26, 32]. Hence, the proposed topology-I in symmetrical configuration requires the least number of devices (switches and DC sources) as compared with conventional and newly developed topologies.

3.2 Comparison of asymmetrical MLI

Comparison of the proposed topology-II with newly developed topologies of [18, 27, 29, 30, 33, 34] and conventional CHB operated in asymmetrical configuration is presented in Figs. 5*c* and *d*. It can be observed that the proposed topology-II requires the least amount of switches in asymmetrical configuration as compared with conventional topology and newly developed topologies. Also, DC source requirement is less as compared with CHB and the newly developed topologies of [18, 27, 29, 30, 34], but requires more sources as the topology of [33] as depicted in Fig. 5*d*.

Fig. 5 proves that the proposed topologies in symmetrical and asymmetrical configurations require the least number of devices (switches and DC sources) as compared with conventional and newly developed topologies. Moreover, the proposed topologies do not require any external circuit for maintaining its capacitor voltage in a balanced state. Table 4 gives the generalised comparison between the proposed topology-I and newly developed topologies for 'N' number of output levels which includes total components required for the single-phase inverter. Table 4 also gives the comparison of various topologies based on total kVA ratings of the switches, which show that the proposed topology has slightly higher (∼6%) kVA rating as compared with CHB and topologies of [27, 30], whereas topologies of [26, 32, 34] have more (∼6%) kVA rating of the switches as compared with the proposed topology.

4 Simulation and experimental results

4.1 Modulation scheme

For controlling the switches, the gate signals are generated by using a suitable multi-carrier pulse-width modulation (MCPWM) technique for both topology-I and topology-II. The carrier switching frequency is kept at 100 Hz and 5 kHz, whereas the reference signal frequency is kept at 50 Hz. In MCPWM technique, the pulses are generated by suitable logical operation between carrier and reference signal and then the pulses are fed to the driver circuit which amplifies the magnitude of generated pulses to trigger the respective switch [43]. In MCPWM technique, the number of carrier signals required is dependent on the number of output levels ('$M-1$'). The basic strategy for MCPWM is given in Fig. 6*a* and gate pulses for the proposed topology-I for 9-level are given in Fig. 6*b*.

4.2 Simulation results

To test and examine the performance of the proposed topologies, a simulation study has been carried out using MATLAB/Simulink. Topology-I is simulated for symmetrical configuration as 9-level inverter and topology-II for the 17-level inverter. Different simulation and experimental parameters for both the topologies are given in Table 5. For calculating the capacitor value, below formula is used:

$$C_S \geq (I_{out} \times t_{on})/(\%\text{ripple} \times V_{in}) \tag{10}$$

where I_{out} is the current delivered by a capacitor, ton is the charging/discharging time of the capacitor, %ripple is the maximum allowable ripple content in capacitor voltage (10% allowance is taken for proposed topologies) and V_{in} is the capacitor balanced voltage.

Fig. 7*a* shows the simulation results of the proposed topology-I for 9-level inverter working in the symmetrical configuration under two different switching frequencies of 5 kHz and 100 Hz, i.e. the switching frequency is suddenly changed from 5 kHz to 100 Hz. Fig. 7*a* depicts the waveforms of the output voltage, output current, capacitor voltage and capacitor current. From Fig. 7*a*, it can be seen that the inverter switching frequency has no impact on capacitor voltage and capacitor maintains its voltage at a balanced state at both the switching frequencies. To examine the performance of the proposed topology-II in asymmetrical configuration, 17-level output waveforms are depicted in Fig. 7*b*. From the waveforms depicted in Fig. 7*b*, it can be seen that the capacitor voltage is in a balanced state at switching frequency of 5 kHz.

To effectively show the self-voltage balancing of its capacitor voltage under sudden load transition, under different modulation index and different reference frequencies, the simulation study is carried out based on 9-level inverter of topology-I and results are given in Figs. 7*c* and *d*. The working of topology-I when the sudden load transition takes place at 0.1 s is shown in Fig. 7*c*. It can be seen from Fig. 7*c* that at 0.1 s the output current increases;

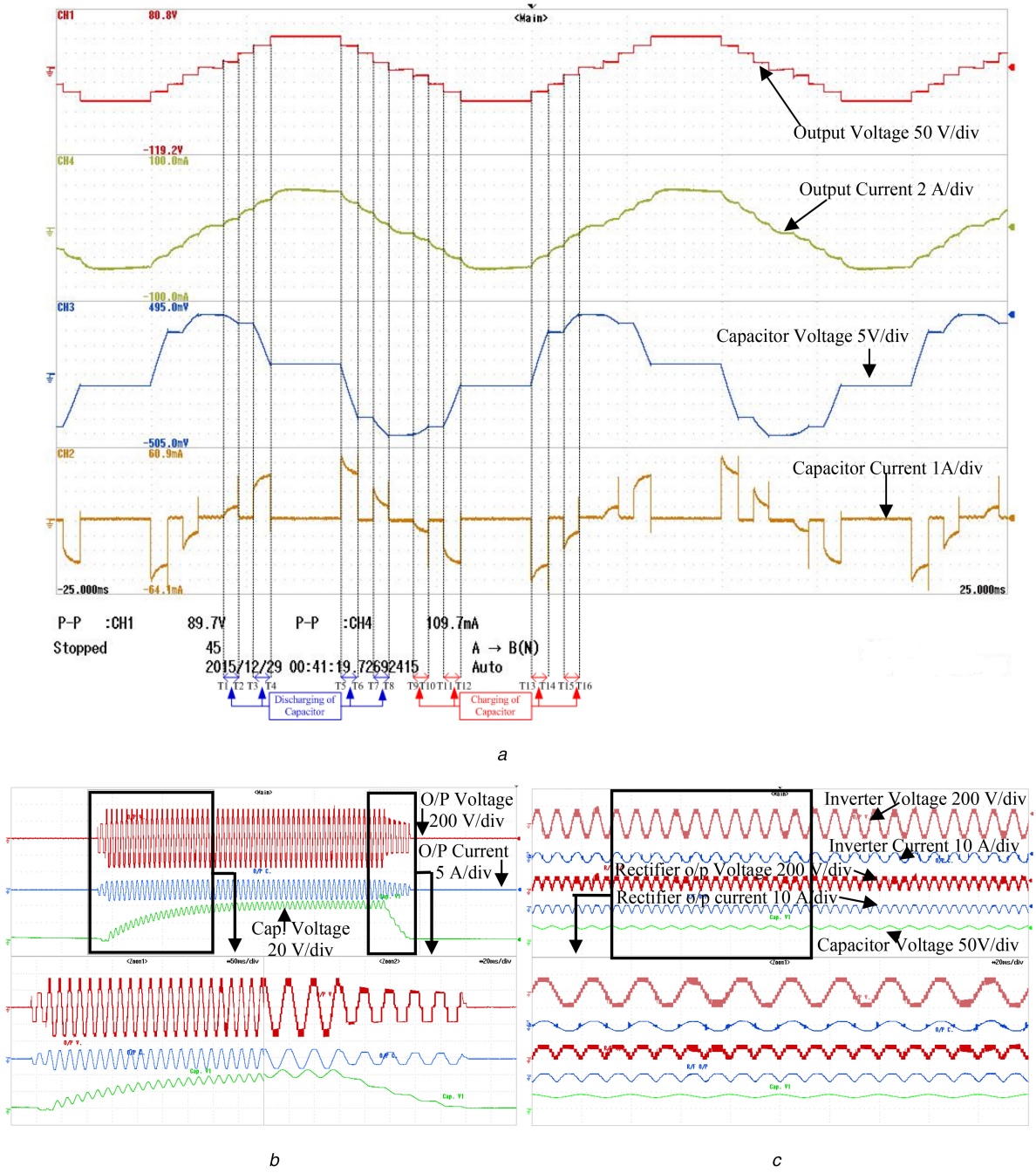

Fig. 4 *Experimental results for demonstrating self-voltage balancing capabilities of the proposed topology*

(a) Charging and discharging phenomenons in the proposed topology, ***(b)*** Switch 'ON' and switch 'OFF' transients, ***(c)*** Working under a non-linear load of diode rectifier

hence, the capacitor current also increases, which results in more ripples in capacitor voltage, but still the voltage remains in a balanced state. The working of topology-I when it is switched from one modulation index to another at 0.1 s is shown in Fig. 7*d*. It can be seen that at 0.1 s when the topology is switched from unity modulation index to 0.5 modulation index the output current decreases due to which capacitor current also decreases, which ultimately results in a decrease in capacitor voltage ripple, but with balanced voltage. Hence from Figs. 7*c* and *d*, it can be said that the capacitor voltage in the proposed topology always remains in a balanced state, regardless of load dynamics, modulation index, switching frequency or reference frequency.

4.3 Experimental results

For precisely testing the working of proposed topologies, a laboratory prototype has been developed for the 9-/17-level inverter of topology-I and topology-II, respectively. For generating the real-time switching pulses, the dSPACE 1103 controller has been used and the generated pulses are then given to gate driver circuit for amplifying the generated pulses and then finally fed to respective switches. The experimental waveforms are analysed by the use of scopecoder YOKOGAWA DL850E. The experimental waveform such as output voltage, output current and capacitor voltages for 9-level proposed topology-I at two different switching frequencies is given in Figs. 8*a* and *b*. Similarly, results for 17-level of topology-II are given in Figs. 8*c* and *d*. From Fig. 8, it is observed that the proposed topology works well at lower as well as at higher switching frequency while maintaining its capacitor voltage in a balanced state for both symmetrical and asymmetrical configurations.

To examine the charging and discharging of the capacitor voltage in the proposed inverter, an experimental study has been carried out for the 9-level inverter and result is given in Figs. 4*a*. From Fig. 4*a*, it can be observed that the average value of the capacitor current is always zero in one complete cycle. Therefore, it is concluded that voltage of the capacitor always remains balanced irrespective of load and modulation index.

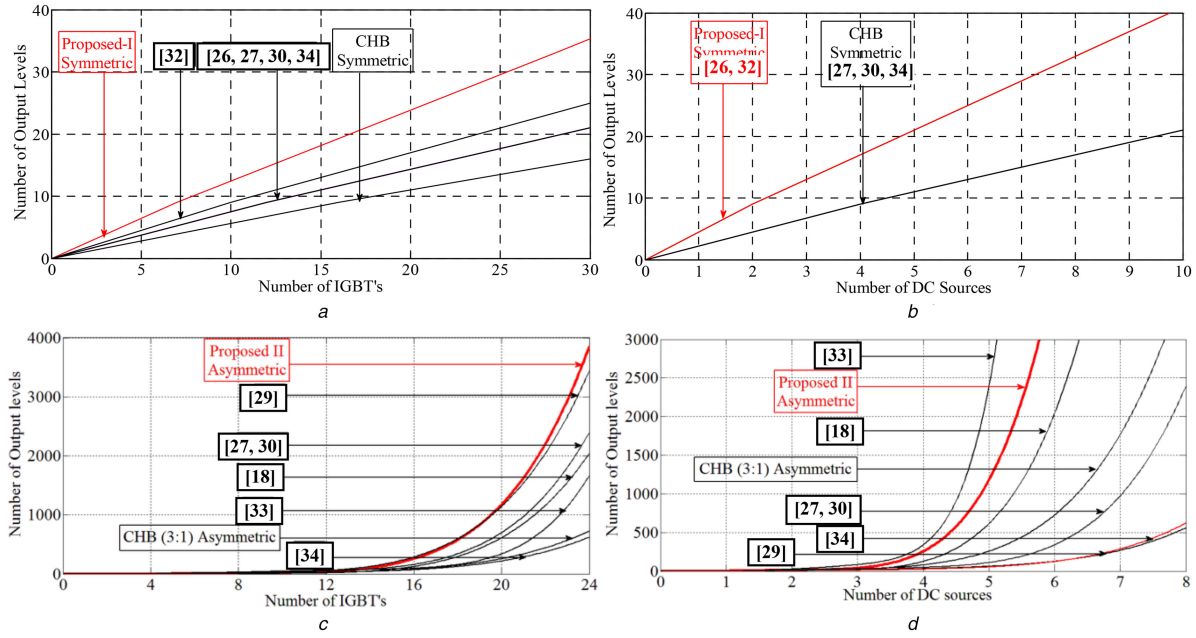

Fig. 5 *Comparison of number of output levels*

(a) Versus number of IGBT's in symmetrical MLI, ***(b)*** Versus number of DC sources in symmetrical MLI, ***(c)*** Versus number of IGBT's in asymmetrical MLI, ***(d)*** Versus number of DC sources in asymmetrical MLI

Table 4 Generalised comparison for single-phase symmetrical MLI

Components	MLI topology								
	Topology-I	CHB	NPC	FC	[26]	[27]	[30]	[32]	[34]
main switches	$(N+19)/4$	$2(N-1)$	$2(N-1)$	$2(N-1)$	$3(N-1)/2$	$3(N-1)/2$	$3(N-1)/2$	$5(N-1)/4$	$3(N-1)/2$
main diodes	$(N+1)$	$2(N-1)$	$2(N-1)$	$2(N-1)$	$7(N-1)/4$	$7(N-1)/2$	$3(N-1)/2$	$2(N-1)$	$3(N-1)/2$
clamping diodes	0	0	$(N-1)\times(N-2)$	0	0	0	0	0	0
DC bus capacitor/ isolated supply	$(N+3)/4$	$(N-1)/2$	$(N-1)/3$	$(N-1)/3$	$(N-1)/2$	$(N-1)/2$	$(N-1)/2$	$3(N-1)/4$	$(N-1)/2$
FC	0	0	0	$(N-1)\times(N-2)/2$	0	0	0	0	0
total number of components	$(1/2)(3N+13)$	$(9/2)\times(N-1)$	$(N-1)\times(3N+7)/3$	$(N-1)\times(3N+20)/3$	$15(N-1)/4$	$11(N-1)/2$	$4(N-1)$	$4(N-1)$	$4(N-1)$
total blocking voltage on the switches ('V_{DC}' as input voltage)	$(17/8)\times(N-1)\times V_{DC}$	$2\times(N-1)\times V_{DC}$	$2\times(N-1)\times V_{DC}$	$2\times(N-1)\times V_{DC}$	$(9/4)\times(N-1)\times V_{DC}$	$2\times(N-1)\times V_{DC}$	$2\times(N-1)\times V_{DC}$	$(9/4)\times(N-1)\times V_{DC}$	$(9/4)\times(N-1)\times V_{DC}$

Also, a theoretical explanation of capacitor voltage balance can be done from Fig. 4*a*. It can be seen that in the positive cycle (i.e. T1–T2, T3–T4, T5–T6 and T7–T8) the capacitor is connected in series with the load, hence discharging phenomenon takes place, whereas in the negative half cycle (i.e. T9–T10, T11–T12, T13–T14 and T15–T16) the capacitor is connected in series with the source and hence charging phenomenon takes place. Now, the time duration of charging and discharging is maintained equal by employing suitable switching strategy. Hence, net energy received is equal to net energy delivered by a capacitor in one complete cycle. Therefore, capacitor voltage always remains in a balanced state.

Fig. 4*b* shows the transient condition during switch 'ON' and switch 'OFF' of the inverter. In Fig. 4*b*, the capacitor voltage initially starts from zero at the switch 'ON' time and settles at half of the input voltage, i.e. 45 V and again goes back to zero at the switch 'OFF' time. It has to be noted that the capacitors used in the proposed topologies take some time to reach the steady-state condition which causes some delay while switching 'ON' the inverter. This kind of delay is also seen in the topologies presented in [35–38] which also uses capacitors to reduce the DC source requirement. In all these topologies, the charging and discharging processes are directly proportional to the load value, i.e. for the lower values of load the capacitor charges quickly and vice versa.

To test the self-voltage balancing capabilities of the proposed inverter, it has been tested experimentally under non-linear loads such as diode rectifier and different load transients and modulation indexes. Fig. 4*c* shows the working of the proposed topology under non-linear load, i.e. diode rectifier. From Fig. 4*c*, it can be said that the capacitor voltage remains in a balanced state under non-linear load. Hence, it is observed that irrespective of load type, modulation index or load dynamics, the capacitor voltage always remains in a balanced state.

4.4 Loss analysis and efficiency

Calculation of losses is very essential part of the system design. MLI undergoes three modes of operations and they are blocking mode, conduction mode and switching mode. In blocking mode, the devices have to withstand the voltage across its terminal, hence no current will flow in this mode across the device due to which the losses in this mode are considered to be negligible. Hence, the majorities of the losses in MLI are in conduction and switching mode

$$P_{\text{Total}} = P_{\text{C}} + P_{\text{SW}} \tag{11}$$

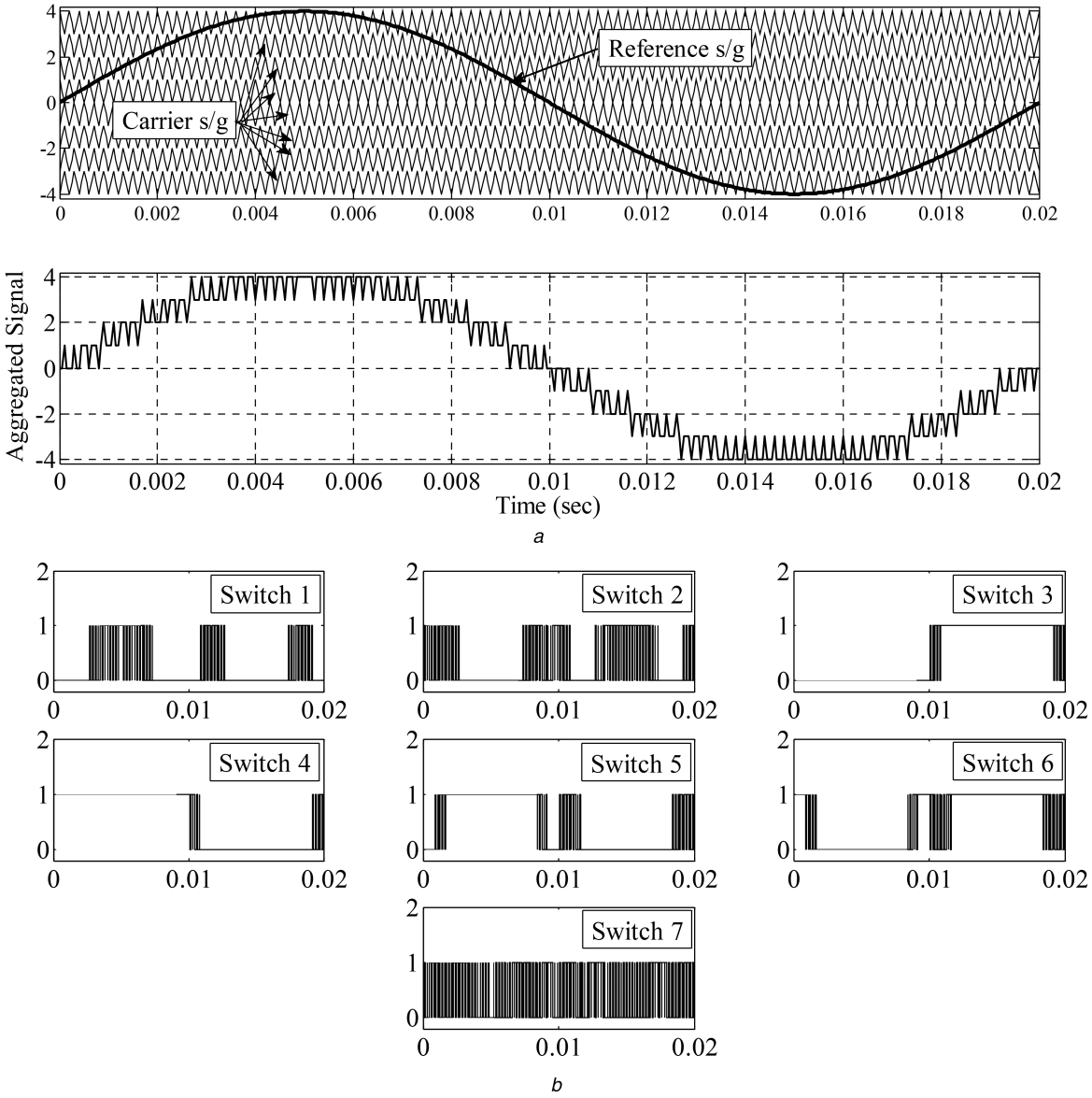

Fig. 6 *Modulation scheme*
(a) Modulation strategies for the 9-level MLI, ***(b)*** Gate pulses for respective switches for 9-level

Table 5 Simulation and experimentation parameters

Parameters	Topology-I for 9-level	Topology-II for 17-level
source-I	90 V	30 V
source-II	90 V	90 V
capacitor, μF	1200	1200
load resistance, Ω	40, 80	40, 80
load inductance, mH	20, 200	20, 200
modulation index	unity, 0.5	unity
switching frequency, Hz	100 and 5000	100 and 5000

where P_{Total} is the total loss, i.e. conduction loss (P_{C}) and switching loss (P_{SW}).

4.4.1 Conduction losses: Conduction mode is described as the amount of power lost when the device is in 'ON' state [44]. In this paper, both diodes and insulated gate bipolar transistors (IGBTs) are used for generating output levels; hence, conduction losses for both the devices are shown. First conduction losses for individual devices are calculated and then generalised to the proposed MLI.

The voltage drop across an IGBT can be written as

$$V_{\text{CE}}(i_{\text{c}}) = V_{\text{CEO}} + r_{\text{c}} \times i_{\text{c}} \tag{12}$$

where 'V_{CEO}' is the forward voltage drop across the IGBT, 'r_{c}' is the internal resistance of IGBT and 'i_{c}' is the collector current. The instantaneous value of IGBT conduction losses is

$$p_{\text{C, T}}(t) = V_{\text{CE}}(t) \times i_{\text{c}}(t) = V_{\text{CEO}} \times i_{\text{c}}(t) + r_{\text{c}} \times i_{\text{c}}^2(t) \tag{13}$$

where '$i_{\text{c}}(t)$' is the instantaneous current. Average losses can be expressed as

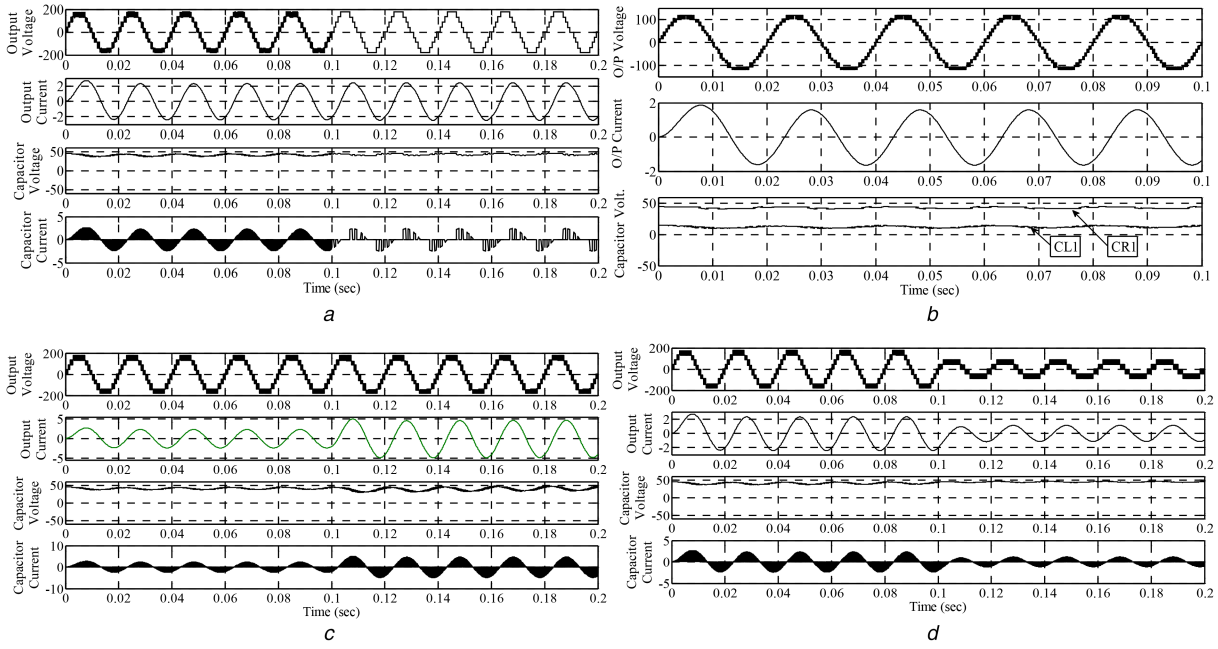

Fig. 7 *Simulation results*

(a) 9-Level waveforms of topology-I at two different switching frequencies of 5 kHz and 100 Hz, ***(b)*** 17-Level waveforms of topology-II at 5 kHz switching frequency, ***(c)*** Sudden load transition, ***(d)*** Sudden change in modulation index, i.e. from unity to 0.5

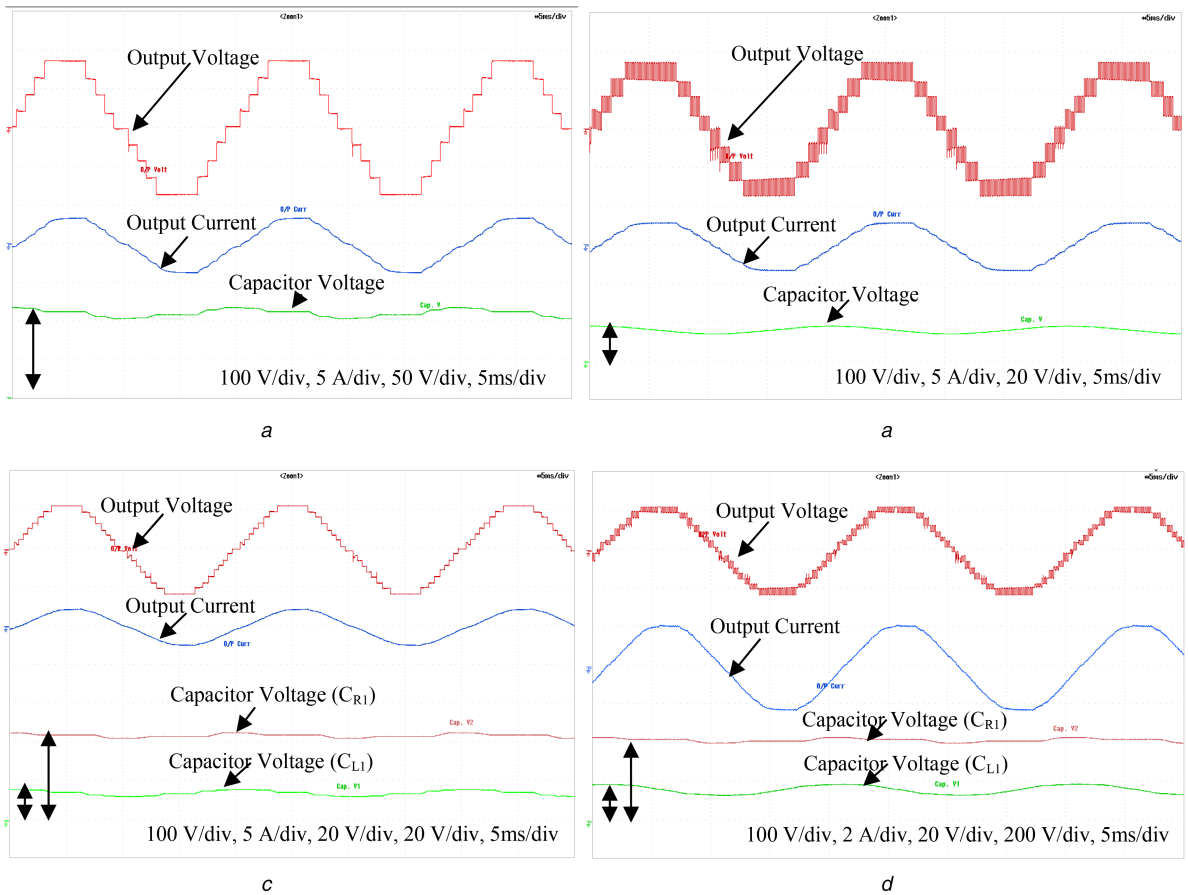

Fig. 8 *Experimental results*

(a) 9-Level waveforms of topology-I at carrier frequency 100 Hz, ***(b)*** 9-Level waveforms of topology-I at carrier frequency 5 kHz, ***(c)*** 17-Level waveforms of topology-II at carrier frequency 100 Hz, ***(d)*** 17-Level waveforms of topology-II at carrier frequency 5 kHz

$$P_{\mathrm{C,T}} = \frac{1}{T_{\mathrm{SW}}}\int_0^{T_{\mathrm{SW}}} p_{\mathrm{C,T}}(t)\,\mathrm{d}t = \frac{1}{T_{\mathrm{SW}}}\int_0^{T_{\mathrm{SW}}} (V_{\mathrm{CEO}} \times i_{\mathrm{c}}(t) + r_{\mathrm{c}} \times i_{\mathrm{c}}^2(t))\,\mathrm{d}t \tag{14}$$

$$P_{\mathrm{C,T}} = V_{\mathrm{CEO}} \times I_{\mathrm{c,av.}} + r_{\mathrm{c}} I_{\mathrm{c,rms}}^2 \tag{15}$$

where '$I_{\mathrm{cav.}}$' is the average value of collector current and '$I_{\mathrm{crms.}}$' is the rms. value of collector current. Similarly, conduction losses for diode can also be approximated as

Table 6 Forward voltage drop and internal resistance of IGBT and diode [45]

Series	Blocking voltage, V	Current capacity, A	IGBT		Diode	
			V_{CEO}, V	r_c, mΩ	V_{DO}, V	r_d, mΩ
FF600R06ME3	600	600	1.9	1	1.95	0.8
FF600R12KE3	1200	600	2.15	1.25	2.5	1
FF500R25KF1	2500	500	3.6	3	2.8	1.4

Table 7 Conduction losses for CHB

Switch number	Conduction losses FF600R06ME3	
	IGBT, W	Diode, W
1	11.543	7.621
2	13.044	0.098
3	5.934	0.489
4	11.886	0.274
5	10.627	2.799
6	13.044	0.098
7	10.619	1.428
8	11.886	0.274
9	9.193	0.900
10	13.044	0.098
11	12.491	2.898
12	11.886	2.224
13	5.458	0.008
14	13.044	0.098
15	12.817	6.686
16	11.888	0.274
total loss	178.406	26.267

Table 8 Conduction losses for the proposed topology-I

Switch number	Conduction losses FF600R06ME3	
	IGBT, W	Diode, W
1	6.509	2.108
2	7.092	2.259
3	25.464	0.099
4	22.800	0.170
5	12.166	1.029
6	14.427	1.755
7	10.847	22.110
total loss	99.304	29.530

$$P_{C,D} = V_{DO} \times I_{D,av.} + r_d I^2_{D,rms} \tag{16}$$

where 'V_{DO}' is the forward voltage drop, 'r_d' is the on-state resistance and '$I_{Dav.}$, I_{Drms}' are the average and root-mean square (RMS) current of diode. For calculating the above-mentioned losses and to draw a suitable comparison between CHB and proposed-I inverter, a MATLAB/Simulink model is built in which data provided in the datasheets are used. Specifications of MATLAB model are:

Total input voltage: 2000 V.
Number of DC sources: four (500 V supplied by each DC source).
Value of resistance: 100 Ω.
Value of inductor: 100 mH.

Table 6 gives the values of the forward voltage drop across IGBT and diode as obtained from datasheets along with its internal resistances for IGBT's of series FF600R06ME3, FF600R12KE3 and FF500R25KF1. Table 7 gives the value of conduction losses for CHB. Table 8 gives the conduction losses for proposed-I inverter.

As can be seen from Tables 7 and 8, conduction losses are more in CHB as compared with proposed-I topology. Conduction losses are *37% (approx.)* less in proposed-I topology for both IGBT and diodes as compared with symmetrical CHB. As seen from Table 8, in the lowest voltage rated switch, i.e. S7, the major losses are in the diode; this is because of the bidirectional switch which consists of one IGBT and four diodes. Hence, most of the losses occur in the diode. The highest voltage rated switches have major losses in IGBT since the conduction through the diode is negligible.

4.4.2 Switching losses: Calculation of switching losses is complex as no simple equation can be found for voltage and current during a switching transient. Switching losses depends on a number of switching transitions, i.e. transition from 'ON' to 'OFF' and transition from 'OFF' to 'ON', blocking voltage, collector current, gate resistance and junction temperature. It also depends on modulation strategy implemented. At first, switching losses are calculated for individual IGBT and diode and then extended for the whole topology. A linear approximation of voltage and current is used for loss calculation. The mathematical expression for calculation of energy loss during turn-off period is

$$E_{off,i} = \int_0^{t_{off}} v(t) \times i(t)\,dt = \int_0^{t_{off}} \left[\left(\frac{V_{B,i}}{t_{off}} \times t\right)\left(-\frac{I}{t_{off}} \times (t - t_{off})\right)\right] dt = 1/6 \times V_{B,i} \times I \times t_{off} \tag{17}$$

where $E_{off,i}$ is the energy loss of the 'ith' switch, $V_{B,i}$ is the blocking voltage of the 'ith' switch, I is the current through the 'ith' switch before turning off and t_{off} is the turn-off time of the 'ith' switch. Similarly, the mathematical expression for calculation of energy loss during turn-on period is

$$E_{on,i} = 1/6 \times V_{B,i} \times I' \times t_{on} \tag{18}$$

where $E_{on,i}$ is the energy loss of the 'ith' switch, $V_{B,i}$ is the blocking voltage of the 'ith' switch, I' is the current through the 'ith' switch after turning ON and t_{on} is the turn-on time of the 'ith' switch. Hence, if assuming $I = I'$, the total switching power losses for individual switch can be calculated as

$$P_{loss,i} = (E_{off,i} + E_{on,i}) \times f_s = \frac{1}{6} \times V_{B,i} \times I \times (t_{on} + t_{off}) \times f_s \tag{19}$$

where f_s is the switching frequency of the 'ith' switch and $P_{loss,i}$ is the power loss for the 'ith' switch. From (19), it is clear that

$$P_{loss,i} \propto V_B \text{ and } P_{loss,i} \propto f_s \tag{20}$$

As earlier discussed that the blocking voltage of the H-bridge switches used in many topologies has been reduced to half in proposed-I topology, hence from (20) it is very clear that the switching losses of the switches of H-bridge reduce to half of the hexagonal cell in proposed-I topology.

To compare the switching losses of 9-level symmetrical CHB with that of 9-level proposed topology-I, (19) can be written as

$$P_{loss} = \frac{1}{6} \times V_B \times I \times (t_{on} + t_{off}) \times f_s \tag{21}$$

Assuming that t_{on} and t_{off} are of same period and they carry the same current I, (21) can be written as

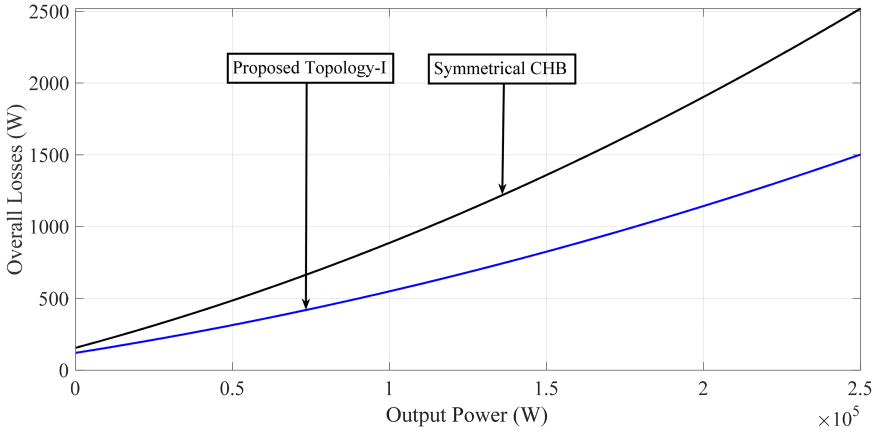

Fig. 9 *Comparison of overall losses on multiple operating points*

$$P_{\text{loss}} = c \times V_{\text{B}} \times f_{\text{s}} \tag{22}$$

where $c = \frac{1}{6} \times I \times (t_{\text{on}} + t_{\text{off}})$ is a constant, thus from (22) switching losses for 9-level symmetrical CHB having voltage source V_{DC} can be written as

$$P_{\text{loss, 9-level CHB}} = 16 \times c \times V_{\text{DC}} \times f_{\text{s}}\,. \tag{23}$$

Now in the proposed topology-I, there is one IGBT with blocking a voltage of V_{DC}, four IGBTs with blocking voltage $2 \times V_{\text{DC}}$ and two IGBTs with blocking voltage $4 \times V_{\text{DC}}$. The two IGBTs with blocking voltage $4 \times V_{\text{DC}}$ are switched only once during a fundamental cycle as discussed earlier. Let the switching frequency be denoted by f_{s} and fundamental frequency be denoted by f_{o}. Then by using (19), switching losses for 9-level proposed inverter-I having voltage source of $2V_{\text{DC}}$ can be written as

$$P_{\text{loss, 9-level Prop-I}} = c \times (V_{\text{DC}} \times f_{\text{s}} + 4 \times 2 \times V_{\text{DC}} \times f_{\text{s}} + 2 \times 4 \times V_{\text{DC}} \times f_{\text{o}}) \tag{24}$$

$$P_{\text{loss, 9-level Prop-I}} = 8 \times c \times V_{\text{DC}} \times \left(\frac{9}{8} \times f_{\text{s}} + f_{\text{o}}\right) \tag{25}$$

Since $\left(\frac{9}{8} \times f_{\text{s}} \gg f_{\text{o}}\right)$, (25) can be written as

$$P_{\text{loss, 9-level Prop-I}} = 9 \times c \times V_{\text{DC}} \times f_{\text{s}} \tag{26}$$

From (23) and (26)

$$P_{\text{loss, 9-level Prop-I}} \cong \frac{P_{\text{loss, 9-level CHB}}}{2} \tag{27}$$

Hence from (27), it is clear that the switching losses of the 9-level proposed inverter-I are almost half as that of 9-level symmetrical CHB under similar operating conditions.

4.4.3 Overall losses: In this section, a comparison has been made between the proposed topology and the conventional CHB based on overall losses and depicted in Fig. 9. For comparison purpose, the simulation results have been taken in which the values provided in datasheets are used for effectively calculating the overall losses. To show the superiority of the proposed topology over conventional CHB, the simulation results have been taken at multiple operating points. From Fig. 9, it can be observed that the proposed topology has lower overall losses as compared with CHB.

5 Conclusion

This paper proposes two new hybrid topologies of symmetrical and asymmetrical MLI with the self-voltage balancing of its capacitor voltage and with a reduced number of devices. For obtaining the maximum number of output levels in asymmetrical configuration, a new algorithm is proposed. The proposed topologies have been tested experimentally for 9-level and 17-level inverters under different switching frequencies. For effectively demonstrating the self-voltage balancing phenomenon of capacitor voltage, the proposed topologies have been tested under non-linear load, reactive load, under different modulation index and different load transition. A wide range of comparison is drawn between the proposed topologies, the conventional and the newly developed topologies which show that the proposed topologies require the least number of switches and DC sources as compared with other topologies.

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